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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,749	04/13/2004	Akio Nakamura	OKI.621	4585

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EXAMINER	
PHAM, HOAI V	
ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,749	NAKAMURA, AKIO	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/21/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-14,16,22-28,31 and 32* is/are pending in the application.

4a) Of the above claim(s) *8-14,16 and 22-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,17-21,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-7, 17-21 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mess et al. [U.S. 2002/0195697] previously applied, in view of Ohie [U.S. Pat. 6,580,164] previously applied, and Chhor et al. [U.S. Pat. 6,843,421] newly cited.

With respect to claim 2, Mess et al. (fig.12A, col. 4) discloses a semiconductor device comprising:

a die pad section (98) having a surface and a back surface;

a first semiconductor chip (60A) having a surface on which a first electrode section (54) is formed, and a back surface fixed to the surface of the die pad section (98);

a second semiconductor chip (60B) having a surface on which a second electrode section is formed, and a back surface fixed to the surface of the first semiconductor chip (60A);

lead terminal sections (102A, 102B) respectively electrically connected to the first and second electrode sections; and

wherein an edge portion of the second semiconductor chip (60B) protrudes from an edge portion of the first semiconductor chip (60A), and an edge portion of the die pad section (98 or 70) protrudes from the edge portion of the first semiconductor chip, and the edge portion of the die pad section (98 or 70) further protrudes from the edge portion of the second semiconductor chip (60B).

Mess et al. does not explicitly disclose an adhesive is disposed on an entirely of the back surface of the second semiconductor chip; a resin encapsulating body that seals the surface and the back surface of the die pad section, and the first and second semiconductor chips.

However, Chhor et al. disclose that it is conventional in the art for the adhesive (91) disposed on an entirely of the back surface of the second semiconductor chip (42a) (see fig. 11, col. 10). Therefore, it would have been obvious to one ordinary skill in the art to have the adhesive as taught by Chhor et al. into the device structure of Mess et al. in order to secure the second semiconductor chip to the first semiconductor chip.

Ohie discloses that it is conventional in the art for a resin encapsulating body (10) that seals the surface and the back surface of the die pad section (8), and the first and second semiconductor chips (103, 113) (see fig. 1 and col. 5, lines 59-67; col. 6, lines 1-17). Therefore, it would have been obvious to one ordinary skill in the art to incorporate the resin encapsulating body as taught by Ohie into the device structure of Mess et al. in order to provide the known purpose of protecting the surface and the back surface of the die pad section, and the first and second semiconductor chips and to allow any heat build up within the second semiconductor chip to transferred downward to the adhesive.

With respect to claim 3, Mess et al. (fig.12A) discloses that the surface of the first semiconductor chip (60A) has first and second sides opposite to each other, the surface of the second semiconductor chip (60B) has third and fourth sides opposite to each other, the surface of the die pad section (98) has fifth and sixth sides opposite to each other, the fourth side of the second semiconductor chip (60B) protrudes from the second side of the first semiconductor chip (60A), and the sixth side of the die pad section (98) protrudes from the fourth side of the second semiconductor chip (60B).

With respect to claim 4, Mess et al. (pp [0057]) discloses that the first and second semiconductor chips (60A and 60B) are substantially identical in shape and size.

With respect to claim 5, Mess et al. (fig. 12A) discloses that a length between the first and second sides of the first semiconductor chip (60A) is defined as a chip length, and a length between the sixth side of the die pad section (98) and the fourth side of the second semiconductor chip (60B) is less than or equal to one-fourth the chip length.

With respect to claim 17, Mess et al. (fig.12A, col. 4) discloses a semiconductor device comprising:

a first semiconductor chip (60A) having a first surface and a second surface opposite to the first surface, and a first electrode section formed on said second surface, said second surface having a first side and a second side opposite to the first side;

a second semiconductor chip (60B) having a third surface fixed onto the second surface, and a fourth surface opposite to the third surface and on which a second electrode section formed on said fourth surface, said fourth surface having a third side and a fourth side opposite to the third side;

a die pad section (98) having a front surface and a back surface, the first semiconductor chip is fixed to said die pad section at a first region of the front surface also including a second region that protrudes from the second side;

lead terminal sections (102A, 102B) respectively electrically connected to the first and second electrode sections; and

wherein the fourth side of the second semiconductor chip protrudes from the second side of the first semiconductor chip, and the second region further protrudes from the fourth side of the second semiconductor chip (60B).

Mess et al. does not explicitly disclose an adhesive is disposed on an entirely of the third surface; a resin encapsulating body that seals the surface and the back surface of the die pad section, and the first and second semiconductor chips.

However, Chhor et al. disclose that it is conventional in the art for the adhesive (91) disposed on an entirely of the third surface (42a) (see fig. 11, col. 10). Therefore, it would have been obvious to one ordinary skill in the art to have the adhesive as taught by Chhor et al. into the device structure of Mess et al. in order to secure the second semiconductor chip to the first semiconductor chip and to allow any heat build up within the second semiconductor chip to transferred downward to the adhesive.

However, Ohie discloses that it is conventional in the art for a resin encapsulating body (10) that seals the surface and the back surface of the die pad section (8), and the first and second semiconductor chips (103, 113) (see fig. 1 and col. 5, lines 59-67; col. 6, lines 1-17). Therefore, it would have been obvious to one ordinary skill in the art to incorporate the resin encapsulating body as taught by Ohie into the device structure of Mess et al. in order to provide the known purpose of protecting the surface and the back surface of the die pad section, and the first and second semiconductor chips.

With respect to claim 18, Mess et al. (pp [0057]) discloses the first and second semiconductor chips (60A and 60B) are substantially identical in shape and size.

With respect to claim 19, Mess et al. (fig. 12A) discloses that a length between the first and second sides of the first semiconductor chip (60A) is defined as a chip length, and a length of the second region, which protrudes from the fourth side of the second semiconductor chip (60B) is less than or equal to one-fourth the chip length.

With respect to claims 6-7 and 20-21, Mess et al. (fig.12A, col. 4) discloses all the limitations as claimed above except the range of the protrudes and the thickness as claimed by Applicant. However, the thickness range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ

233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claims 31-32, Mess et al. (fig.12A) discloses that the first and second semiconductor chips (60A and 60B) are disposed so as to be contained within a perimeter of the surface of the die pad section (98).

Response to Arguments

3. Applicant's arguments with respect to claims 2-7, 17-21, 31 and 32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

5. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hoai v Pham/
Primary Examiner, Art Unit 2814